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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,555	09/12/2003	Mitsuaki Izuha	04329.3139	6394

7590 10/06/2004

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,555	IZUHA ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of group I (claims 1-6) in the reply filed on 07/20/04 is acknowledged.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,737,324 to Chang.

Regarding claim 1, Chang (figures 2A-F) teaches a semiconductor device having a MOSFET, the MOSFET comprising:

source (208) and drain (208) regions formed in a major surface region of a semiconductor substrate (200);

a gate insulating film (202) formed on channel region between the source (208) and drain (208) regions;

gate electrode (212) which is formed on the gate insulating film (202) and includes a poly-Si_{1-x}-Ge_x layer (SiGe);

first metal silicide film (216) which is formed on the gate electrode (212) and consists of NiSi; and

second (216) and third (216) metal silicide films which are formed on the source (208) and drain (208) regions, respectively and consist of NiSi.

Chang differs from the claimed invention by not showing the poly-Si_{1-x}-Ge_x layer having a Ge/(Si+Ge) composition ratio x ($0 < x < 0.2$). It would have been obvious to one having ordinary skill in the art at the time the invention was made for the poly-Si_{1-x}-Ge_x layer having a Ge/(Si+Ge) composition ratio x ($0 < x < 0.2$) because it is a used material for the gate electrode. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 2, Chang differs from the claimed invention by not showing the Ge/(Si+Ge) composition ratio more preferably falls within a range of $0.04 \leq x \leq 0.16$. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the Ge/(Si+Ge) composition ratio more preferably falls within a range of $0.04 \leq x \leq 0.16$ because it is a used material for the gate electrode. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 5, Chang differs form the claimed invention by not showing a thickness of the poly-Si_{1-x}-Ge_x layer in the gate electrode is at least twice that of the first metal silicide film. It would have been obvious to one having ordinary skill in the art at the time the invention was made for a thickness of the poly-Si_{1-x}-Ge_x layer in the gate electrode is at least twice that of the first metal silicide film because it reduces the resistivity of the gate electrode. Furthermore, it

has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

3. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang in view of US Patent No. 6,063,680 to Wu and US Patent No. 6,288,430 to Oda.

Regarding claim 3, the disclosures of Chang are discussed as applied to claims 1, 2 and 5 above.

Chang differs form the claimed invention by not showing the first metal plug, which is formed in a first contact hole formed in the interlayer dielectric film on the gate electrode, the second and third plugs, which are formed in the second and third contact holes formed in the interlayer dielectric on the source and drain regions. However, Wu (figures 1-10) teaches the first metal plug (34), which is formed in a first contact hole formed in the interlayer dielectric film (32) on the gate electrode (12), the second (34) and third (34) plugs, which are formed in the second and third contact holes formed in the interlayer dielectric (32) on the source and drain regions. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Wu into the device taught by Chang because the contact plugs provide interconnections between the device and the external device. The combined device shows the first metal plug, which is formed in a first contact hole formed in the interlayer dielectric film on the gate electrode, the second and third plugs, which are formed in the second and third contact holes formed in the interlayer dielectric on the source and drain regions.

Chang and Wu differ from the claimed invention by not showing a first barrier metal layer which is inserted between the first metal plug and the first metal silicide film, and second and third barrier metal layers which are inserted between the second and third metal plugs and the second metal silicide film. However, Oda (figure 16) teaches the barrier layer (14 or 34) formed around the contact holes (33). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Oda into the device taught by Chang and Wu because there is no contamination of dielectric material with metal layer occurs. The combined device shows a first barrier metal layer, which is inserted between the first metal plug and the first metal silicide film, and second and third barrier metal layers, which are inserted between the second and third metal plugs and the second metal silicide film.

Regarding claim 4, the combined device shows the first to third barrier metal layers contain TiN (Oda; TiN barrier layers), and the first to third metal plugs consist tungsten (Wu; column 4, lines 17-18).

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,737,324 to Chang in view of US Patent No. 5,427,964 to Kaneshiro et al.

Regarding claim 6, Chang differs from the claimed invention by not showing a well region, which is formed in the semiconductor substrate. However, Kaneshiro et al. (figure 1) teach a well (13), which is formed in the semiconductor substrate (11). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Kaneshiro et al. into the device taught by Chang because of the

advantage of the increased breakdown voltage and isolation resulting from the additional well. The combined device shows a well region which is formed in the semiconductor substrate, and in which the source and drain regions are formed in the well region, the source and drain regions have structures with source and drain extensions, and first and second heavily doped impurity diffusion regions and third and fourth lightly doped impurity diffusion regions formed near the channel region the first and second impurity diffusion regions.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
September 30, 2004

DONGHEE KANG
PRIMARY EXAMINER